IN THE SPECIFICATION

Please amend the below listed paragraphs of the specification as shown.

[0017] FIGS. 1 and 2 are sets of electrical schematic diagrams which model the impedance of a theoretical two-branch switching path according to conventional practice (FIG. 1), and according to a cascaded method used in accordance with embodiments of the present invention (FIG. 2). In FIGS. 1 and 2, one branch 11 of illustrated switch is in an ON state, permitting a signal to pass from an input 12 to an output 14. The other branch 15 leads to an output 16. Both topologies are constructed of insulated gate field effect transistors (IGFETs). In FIG. 1, a two-branch switch indicated generally at 10 has a first branch 11 which includes two FET switches 13 and 20, here modeled as resistances with a value R. The other branch 15 has two FETs 17 and 22, which in their OFF state have dominating junction capacitances C. As shown in the first simplification, branch 11 has an equivalent resistance 2R while branch 15 has an equivalent junction capacitance C/2. Simplifying by one more step, this is approximated by an overall insertion loss 21 of 2R.

[0022] In the illustrated embodiment, the integrated circuit 100 includes a single pole, three throw (SP3T) switching section 102, the boundaries of which are shown in dotted and dashed line. In FIG. 5, the signal paths are shown in solid line while the switching control signal paths are shown in dotted line. Switching section 102 includes a switch 104 which is operable by control line ~~VTx2~~ VTx1 to connect transmitter port Tx1 to the antenna port ANT. A similar switch 106 is operable by switching signal VTx2 to connect transmitter port Tx2 to the antenna port ANT. A switch 108 is a first stage in a cascaded switching system and is operable by a receiver switching signal VRxC to connect a receiver signal node 110 to the antenna port ANT. While, in the illustrated embodiment, the integrated circuit 100 selectively switches one of two transmitter ports, the invention also contemplates embodiments having one or three or more transmitter ports.

[0025] FIG. 6 shows an exemplary layout and topography of an integrated switching circuit similar to that shown in FIG. 5. The FETs for switching transmitter signals Tx1 and Tx2 are shown at 102, while the receiver switching section is shown at 112. Each of the series switching FETs are high-power interdigitated switching transistors in which the sources and drains each have a plurality of fingers that are interleaved with each other. The interdigitated sources and drains ~~maybe~~ may be created by suitable implants of a first conductivity type into a semiconductor substrate having an opposite conductivity type, and the implants may be self-aligned to the gates which are disposed between them. In the illustrated embodiment, the gates are sinuous metallizations, but in alternative embodiments the gates can be branched instead. The shapes of the channels of course correspond to the gates.

[0027] In operation and referring to FIG. 5, the integrated circuit in the illustrated embodiment can operate in either of two transmission modes or any of four receiver modes. If, for example, a signal is to be transmitted from pad Tx1, VTx1 will be high, and VTx2, VRxC, VRx2, VRx1, VRx3 and VRx4 will be low. This turns on series transistor topology 104 ~~on~~, and turns all other switching transistors off. In this condition the series transistor topology 104 will contribute a relatively low resistance to the insertion loss and the junction capacitance of the other, OFF branches of the circuit contribute little to the sensed impedance.

[0029] In summary, a single-die integrated circuit has been shown and described in FIGS. 5 and 6 which can be used to switch a plurality of wireless signals to and from an antenna. The described IC arranges its switching FETs in a cascaded topology, as is illustrated in FIGS. 2 and 4, in order to reduce insertion loss in the strength of the switched signals. This reduced insertion loss resulting from the cascaded topology enables a single die design in which receiver and transmission ports appear on the same die. In contrast, prior art IC's that arrange

~~its~~ their switching FETs using a conventional topology, as shown in FIGS. 1 and 3, are required to provide receiver and transmission portions on separate dies, to avoid insertion loss and high capacitive loading. The integrated circuit in accordance with embodiments of the present invention is useful for switching signals in CDMA, w-CDMA, IEEE 802.11, Bluetooth and like wireless protocols and saves space in comparison to chips which handle transmission or reception alone. While preferred embodiments of the present invention have been illustrated in the appended drawings and described in the detailed description above, the present invention is not limited thereto but only by the scope and spirit of the appended claims.